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CREATIVE IN TAIWAN

# Software Proxy Memory Interface

SIGNAL, HARDWARE ARCHITECTURE, PACKAGE, COMMAND SET,  
OPERATION TIME, AND TIMING DIAGRAM

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# Software Proxy Memory Interface

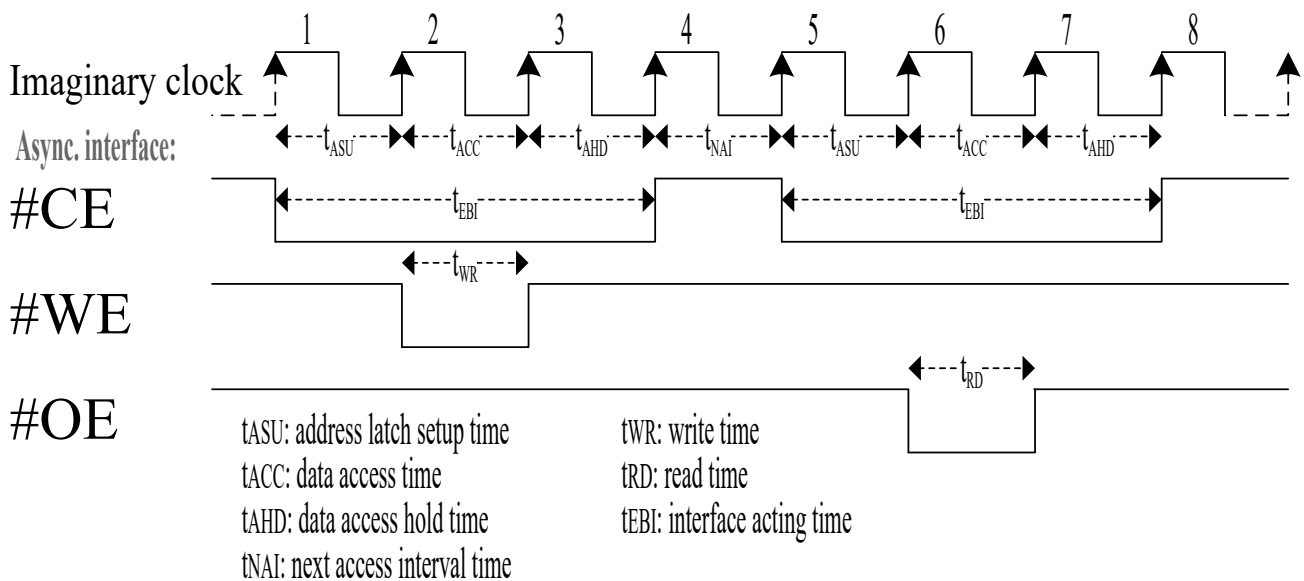
*A software program executing in the microprocessor, it works in coordination with the external bus interface (EBI) or the internal interconnect bus to access and control various memories. The memory comprises DRAM and the flash memory. The software program can be a firmware, a microcode, or implemented in the FPGA.*

## Software Proxy Memory Interface (SPMI)

### ■ The technical terms of major EBI signals:

A[a]	address bus, said 'a' is address width
D[d]	data bus, said 'd' is data width
#CS; #CE	chip selection on the host side; chip enable on the device side
#WE	write enable
#OE	output enable

## Timing Diagram of EBI



$$t_{EBI} = t_{ASU} + t_{ACC} + t_{AHD}$$

$$Access\ Speed = t_{EBI} + t_{NAI}$$

$$Bus\ Frequency = \frac{1}{Access\ Speed} \parallel Bus\ Frequency \leq 200MHz$$

### ■ The time parameters for DRAM:

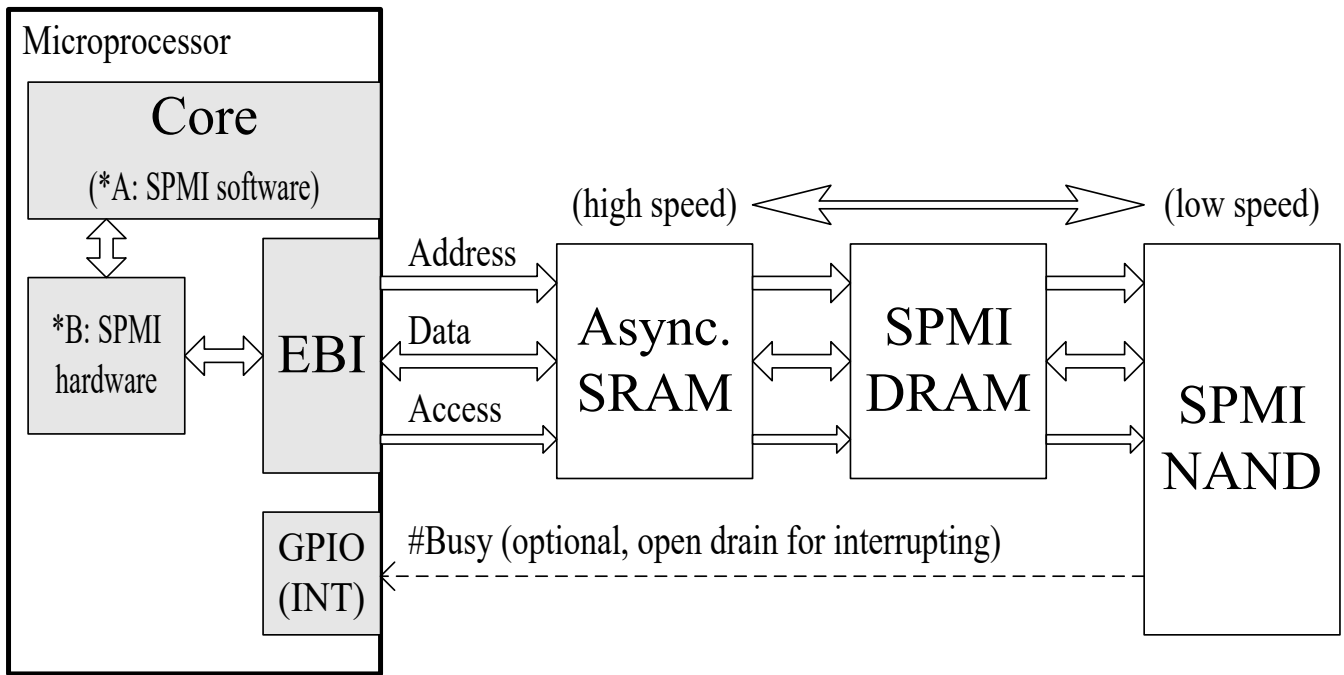
Data Retention Time on the Cell: tDRC

Average Periodic Refresh Interval: tREFI (refer to DDR-n SDRAM specification)

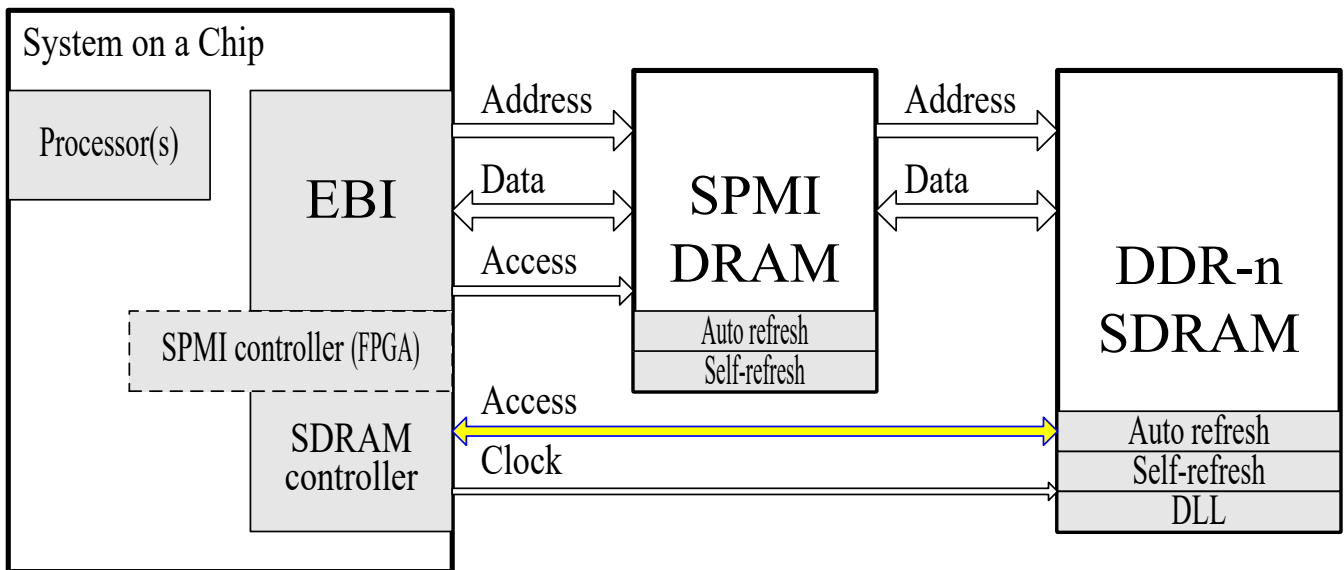
Refresh Cycle Time: tRFC (refer to DDR-n SDRAM specification)

Write One Latency: WOL

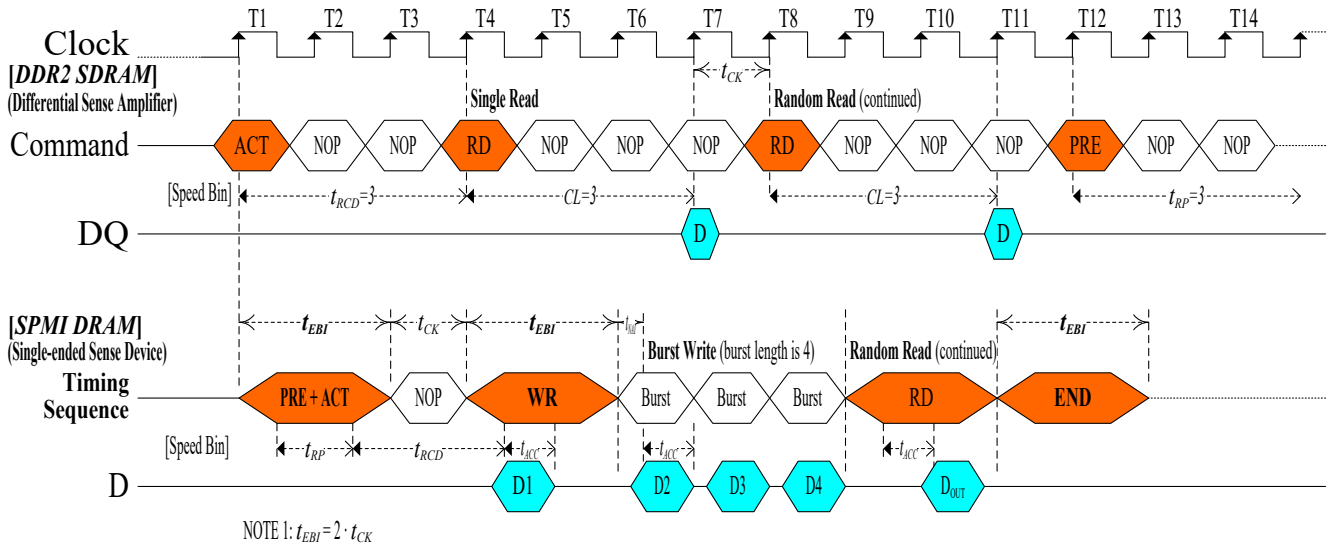
Platform Hardware Architecture



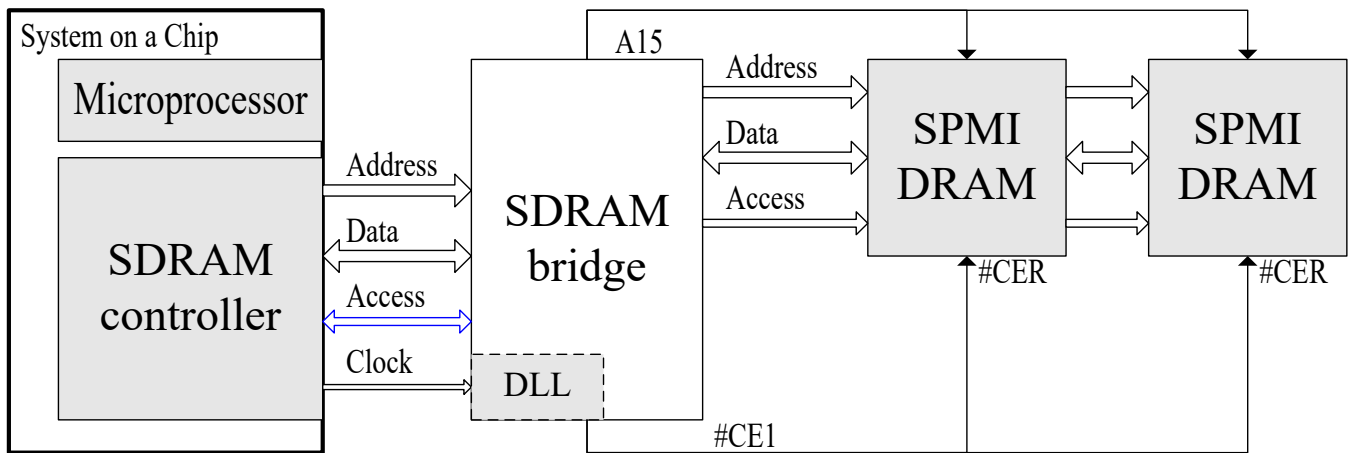
SPMI DRAM versus DDR-n SDRAM



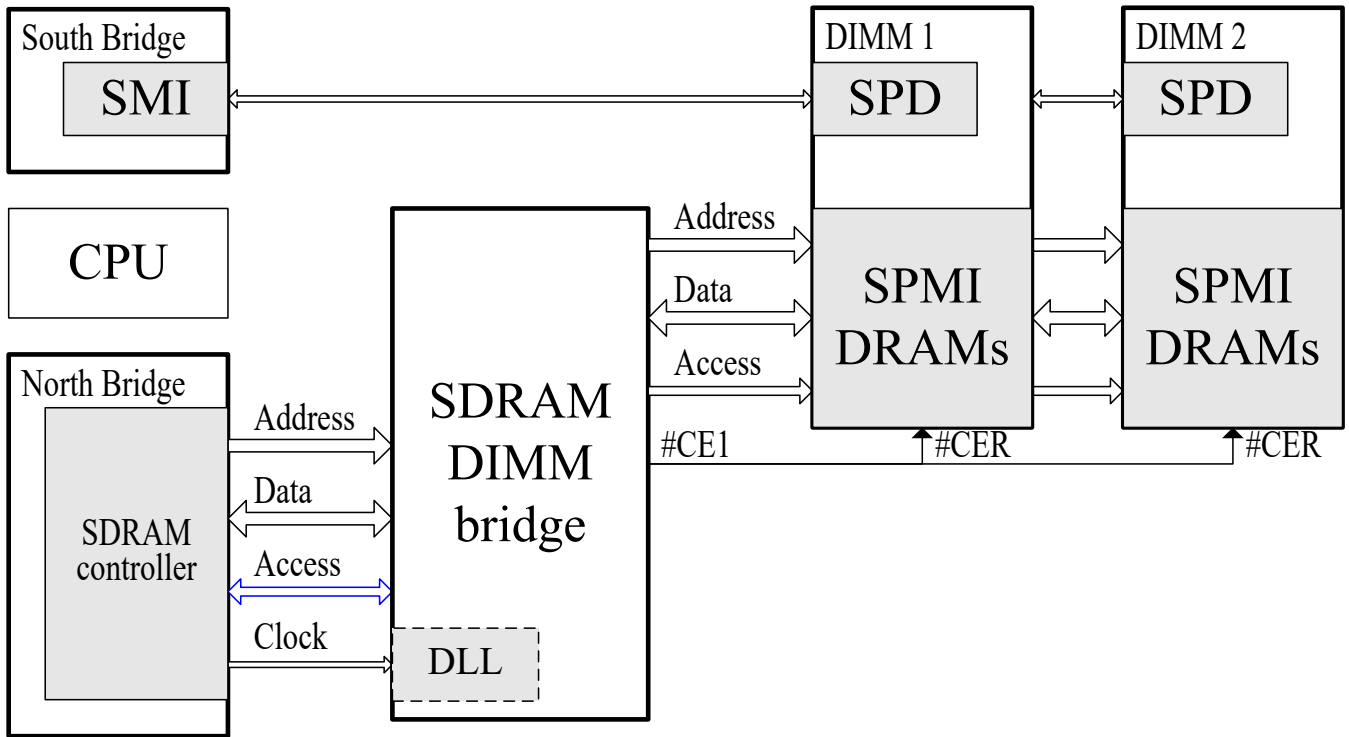
### SPMI DRAM versus DDR2 SDRAM



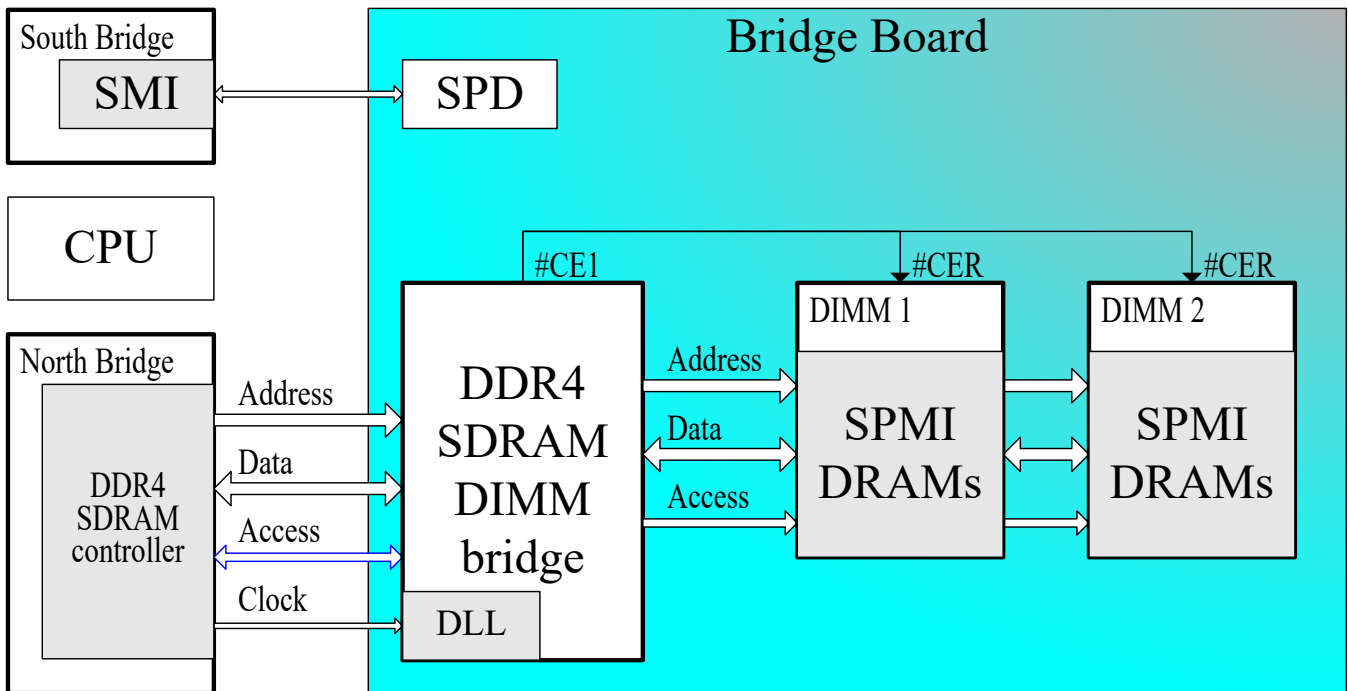
### SDRAM Bridge: hardware platform of SoC



SDRAM DIMM Bridge: hardware platform of X86 personal computer



SDRAM DIMM Bridge Board: hardware platform of X86 personal computer



## Package Ball-out

## DDR2 SDRAM package mapping table

The package ball-out please refer to “JEDEC STANDARD, DDR2 SDRAM SPECIFICATION”.

## Input/output of DDR2 SDRAM interface on the device side, and mapping to SPMI

Symbol of DDR2 SDRAM	Type of DDR2 SDRAM	Symbol of SPMI DRAM	Type of SPMI DRAM	Symbol of SPMI NAND	Type of SPMI NAND
A0—A15 (address bus)	Input	A0—A15 (address bus)	Input	A0—A15 [AD0—AD15]	Input [Input / Output]
DQ (data bus)	Input / Output	D (data bus)	Input / Output	D [reserved]	Input / Output
BA0—BA2 (bank address)	Input	(reserved)		A16—A18	Input
CK, #CK	Input	(reserved)		(reserved)	Input
CKE	Input	(reserved)		<b>ALE</b>	Input
#CS	Input	#CE	Input	#CE	Input
DM	Input	#OE	Input	#OE	Input
#WE	Input	#WE	Input	#WE	Input
#RAS	Input	#CER	Input	(reserved)	
#CAS	Input	(reserved)		#Busy	Output (open drain)
ODT	Input	EtST (self-test entry)	Input	EtST (self-test entry)	Input
[#UDQS]	Input / Output	[#UB]	Input	[#UB]	Input
[#LDQS]	Input / Output	[#LB]	Input	[#LB]	Input
V <sub>REF</sub>	Supply	[V <sub>PP</sub> ]	Supply	[V <sub>PP</sub> ]	Supply
V <sub>DDQ</sub>	Supply	V <sub>DDQ</sub>	Supply	V <sub>DDQ</sub>	Supply
V <sub>SSQ</sub>	Supply	V <sub>SSQ</sub>	Supply	V <sub>SSQ</sub>	Supply
V <sub>DD</sub>	Supply	V <sub>DD</sub>	Supply	V <sub>DD</sub>	Supply
V <sub>SS</sub>	Supply	V <sub>SS</sub>	Supply	V <sub>SS</sub>	Supply

## Input/output of SPMI DRAM on the device side, and mapping to EBI DRAM

Symbol of SPMI DRAM	Type of SPMI DRAM	Symbol of EBI DRAM	Type of EBI DRAM
A0—A15 (address bus)	Input	AD0—AD15 (address and data bus)	Input / Output
D (data bus)	Input / Output	(reserved)	
(reserved)		(reserved)	
(reserved)		(reserved)	
(reserved)		ALE	Input
#CE	Input	#CE	Input
#OE	Input	#OE	Input
#WE	Input	#WE	Input
#CER	Input	(reserved)	
(reserved)		(reserved)	
EtST (self-test entry)	Input	EtST (self-test entry)	Input
[#UB]	Input	#UB	Input
[#LB]	Input	#LB	Input
[V <sub>PP</sub> ]	Supply	[V <sub>PP</sub> ]	Supply
V <sub>DDQ</sub>	Supply	V <sub>DDQ</sub>	Supply
V <sub>SSQ</sub>	Supply	V <sub>SSQ</sub>	Supply
V <sub>DD</sub>	Supply	V <sub>DD</sub>	Supply
V <sub>SS</sub>	Supply	V <sub>SS</sub>	Supply



## DDR3 SDRAM package mapping table

The package ball-out please refer to “JEDEC STANDARD, DDR3 SDRAM SPECIFICATION”.

### Input/output of DDR3 SDRAM interface on the device side, and mapping to SPMI

Symbol of DDR3 SDRAM	Type of DDR3 SDRAM	Symbol of SPMI DRAM	Type of SPMI DRAM	Symbol of SPMI NAND	Type of SPMI NAND
A0—A15 (address bus)	Input	A0—A15 (address bus)	Input	A0—A15 [AD0—AD15]	Input [Input / Output]
DQ (data bus)	Input / Output	D (data bus)	Input / Output	D [reserved]	Input / Output
BA0—BA2 (bank address)	Input	(reserved)		A16—A18	Input
CK, #CK	Input	(reserved)		(reserved)	Input
CKE	Input	(reserved)		<b>ALE</b>	Input
#CS	Input	#CE	Input	#CE	Input
DM	Input	#OE	Input	#OE	Input
#WE	Input	#WE	Input	#WE	Input
#RAS	Input	#CER	Input	(reserved)	
#CAS	Input	(reserved)		#Busy	Output (open drain)
ODT	Input	EtST (self-test entry)	Input	EtST (self-test entry)	Input
[#DQSU]	Input / Output	[#UB]	Input	[#UB]	Input
[#DQSL]	Input / Output	[#LB]	Input	[#LB]	Input
V <sub>REFDQ</sub> , V <sub>REFCA</sub>	Supply	[V <sub>PP</sub> ]	Supply	[V <sub>PP</sub> ]	Supply
V <sub>DDQ</sub>	Supply	V <sub>DDQ</sub>	Supply	V <sub>DDQ</sub>	Supply
V <sub>SSQ</sub>	Supply	V <sub>SSQ</sub>	Supply	V <sub>SSQ</sub>	Supply
V <sub>DD</sub>	Supply	V <sub>DD</sub>	Supply	V <sub>DD</sub>	Supply
V <sub>SS</sub>	Supply	V <sub>SS</sub>	Supply	V <sub>SS</sub>	Supply

## SPMI DRAM

Applying to a high performance dynamic random-access memory.

Parameters of speed bin: tRCD (row to column delay time), tACC (access time)

### ■ Symbols

Address width of bank: b

Address width of row: r (r≤14)

Address width of column: c (c<r)

Mount of storage cell: n

## Operation Time of Accessing and Refreshing

### ■ The device refresh parameters

tDRC: decided by the struct of the storage cell, the process technology, and the 'n'

$$t_{REFI} = \frac{t_{DRC}}{n = 2^x, x \geq 7} \text{ (all bank refresh)}$$

$$t_{RFC} = t_{RP} + t_{RCD}^{REF} [t_{RCD}^{REF} \geq t_{RCD}]$$

### ■ The time of random access (tRACC) with data amount (DA)

$$t_{RACC} = t_{RCD} + t_{NAI} * DA + t_{EBI} * (2 + DA)$$

### ■ The time of burst access (tBACC) with data amount (DA)

$$t_{BACC} = t_{RCD} + t_{NAI} * DA + t_{EBI} * 3 + t_{ACC} * (DA - 1)$$

## Command Set

Function	A[15:14]	A[r-1:0]	D[7:0]
Data Access	01	Column Address* <sup>1</sup>	Byte
Single Bank Precharge, Random Access	01	Row Address	Bank Address
Single Bank Precharge, Synchronization Burst Access* <sup>2</sup>	01	Row Address	Bank Address
Function End	00	X	X
Read Chip Information	00	Page Number* <sup>3</sup>	V (hardware fixed)
Write Chip Configuration	00	Page Number* <sup>3</sup>	V (power on reset)
Auto Refresh* <sup>4</sup> (all bank)	1X	Activating #CER	

NOTE 1: the device first receives the row address, and then receives the column address (A[c-1:0]) after.

NOTE 2: rolling column address.

NOTE 3: using A[1:0] only.

NOTE 4: several #CER (#CE for refresh) connect to same #CE to be a refresh group.

**Chip Information**

D[7:5]	D[4:3]	D[2:1]	D[0]	A[1:0]
<b>Number of banks</b>	<b>Pins of row</b>	<b>Width of column</b>	<b>Wafer process</b>	<b>Info. Page</b>
000: 2	00: 11	00: 10	0: DRAM process	00: page 0
001: 4	01: 12	01: 11	1: logic process	
010: 8	10: 13	10: 12		
011: 16	11: 14	11: 13		
100: 32				
101: 64				
110: 128				
111: 256				

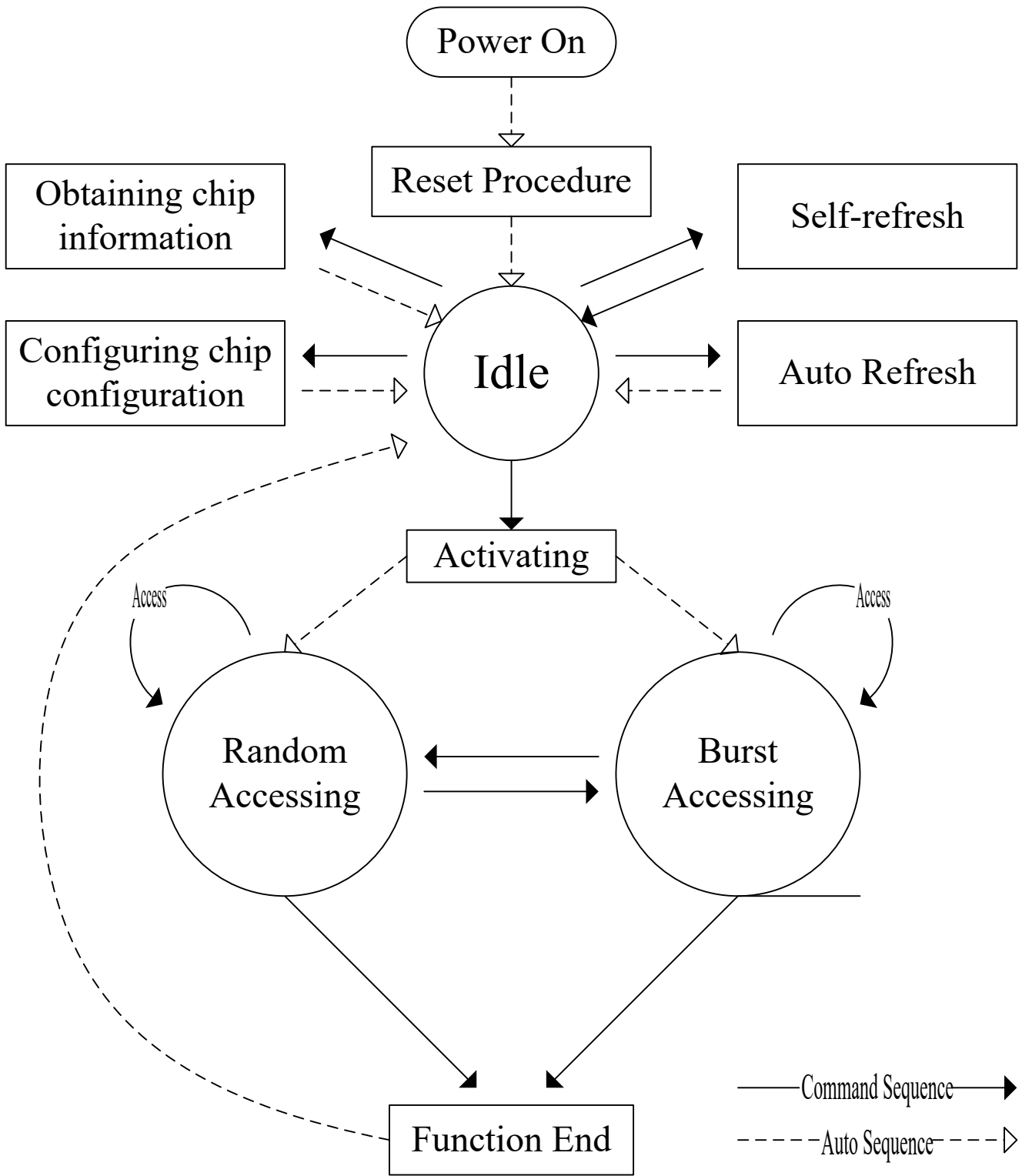
D[7:6]	D[5:2]	D[1:0]	A[1:0]
<b>Mount of storage cell</b>	<b>tRFC (typical)</b>	<b>tNAI (typical)</b>	<b>Info. Page</b>
00: 128	XXXX: from 1ns to 16ns	00: 0.25ns	01: page 1
01: 256		01: 0.5ns	
10: 512		10: 1ns	
11: 1024		11: 2ns	

D[7:5]	D[4:2]	D[1:0]	A[1:0]
<b>tRCD (typical)</b>	<b>tACC (typical)</b>	<b>tREFI (typical)</b>	<b>Info. Page</b>
XXX: from 1ns to 8ns	000: 0.5ns	00: 4us	10: page 2
	XXX: from 1ns to 7ns	01: 2us	

**Chip Configuration**

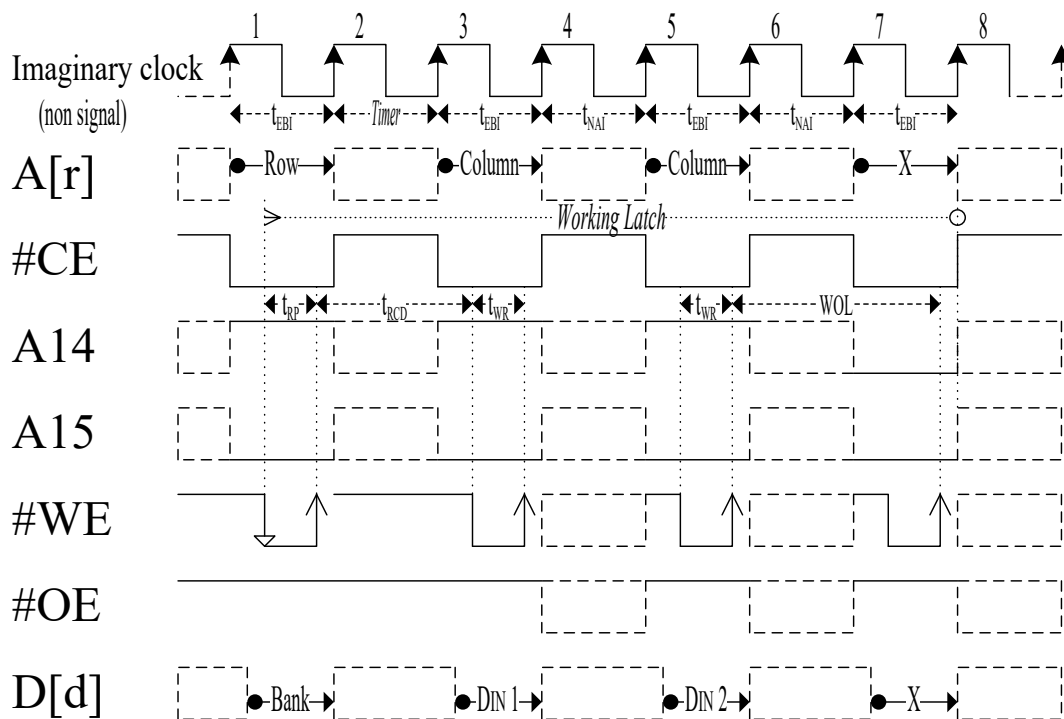
D[7:1]	D[0]	A[1:0]
<b>Null</b>	<b>Self-refresh</b>	<b>Config page</b>
0	0: exit (POR)	00: page 0
	1: entry	

Simplified State Diagram

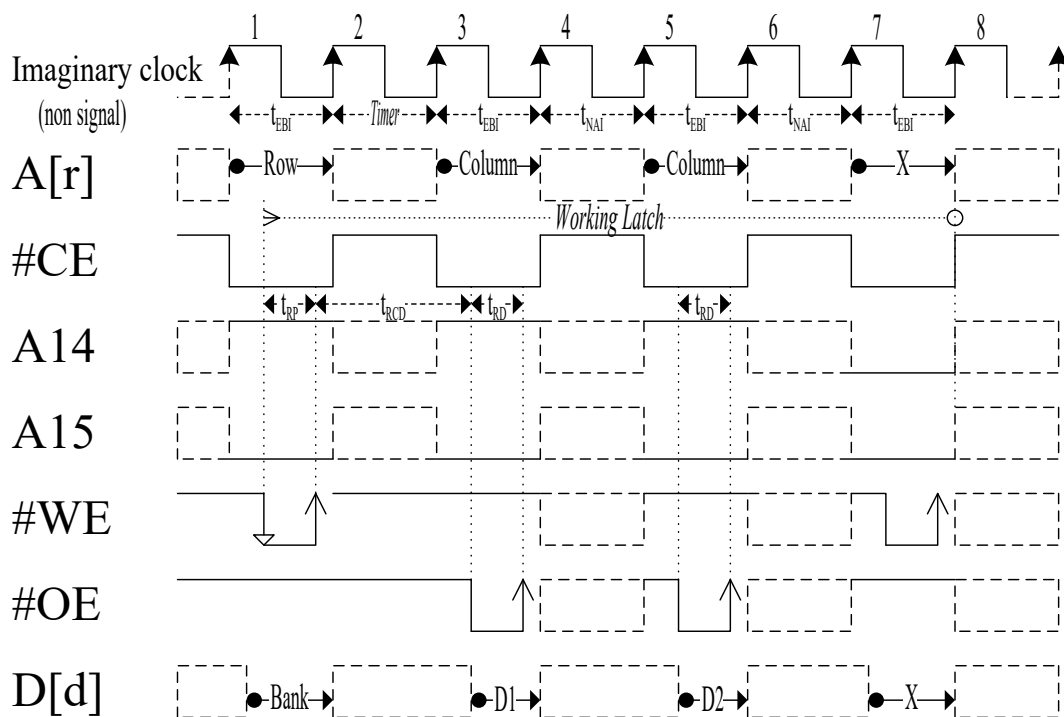


## Timing Diagram

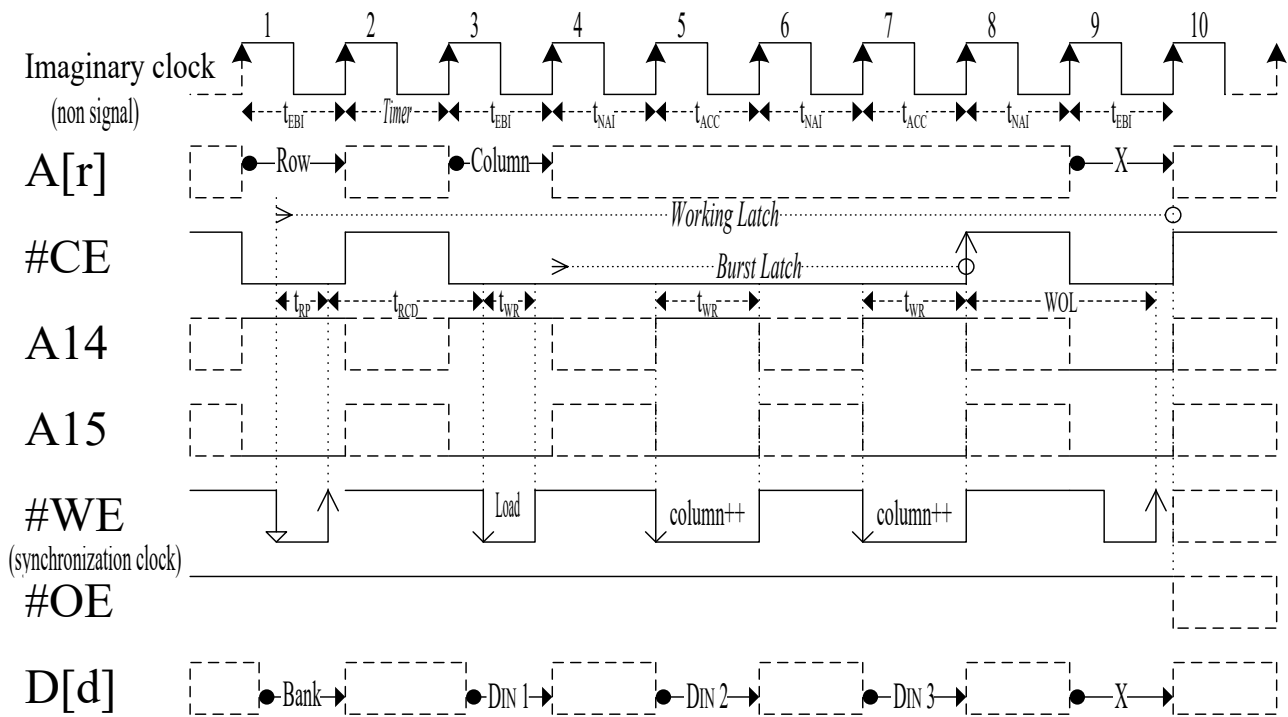
### ■ Random Write



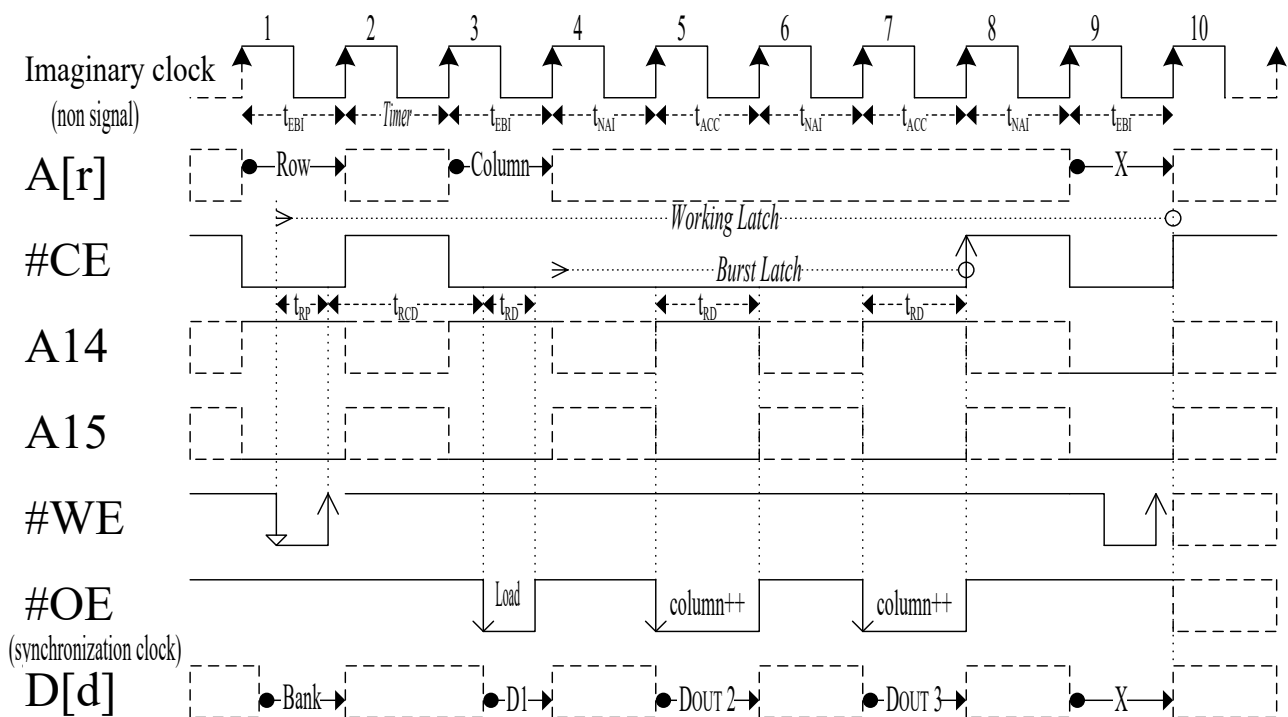
### ■ Random Read



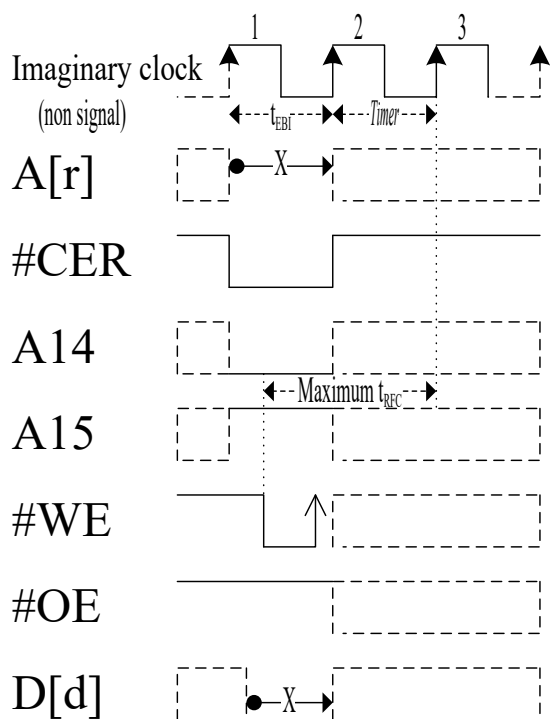
■ Synchronization Burst Write



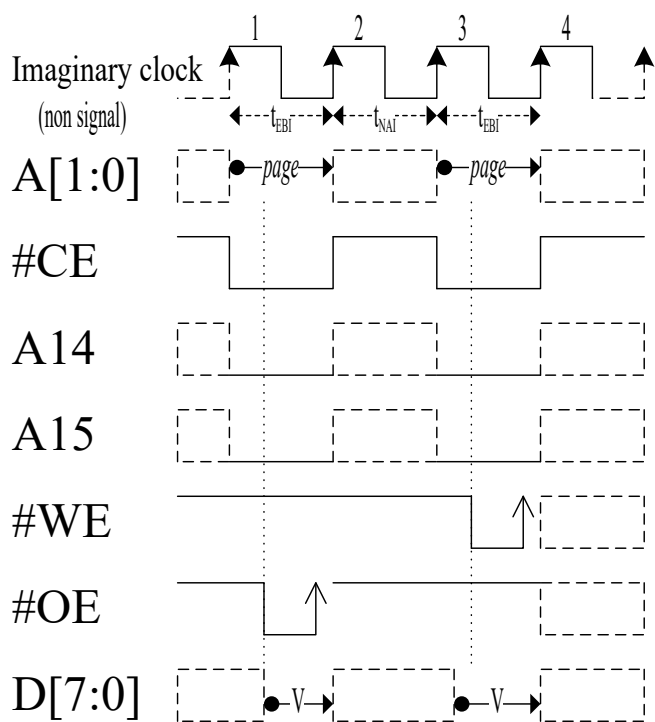
■ Synchronization Burst Read



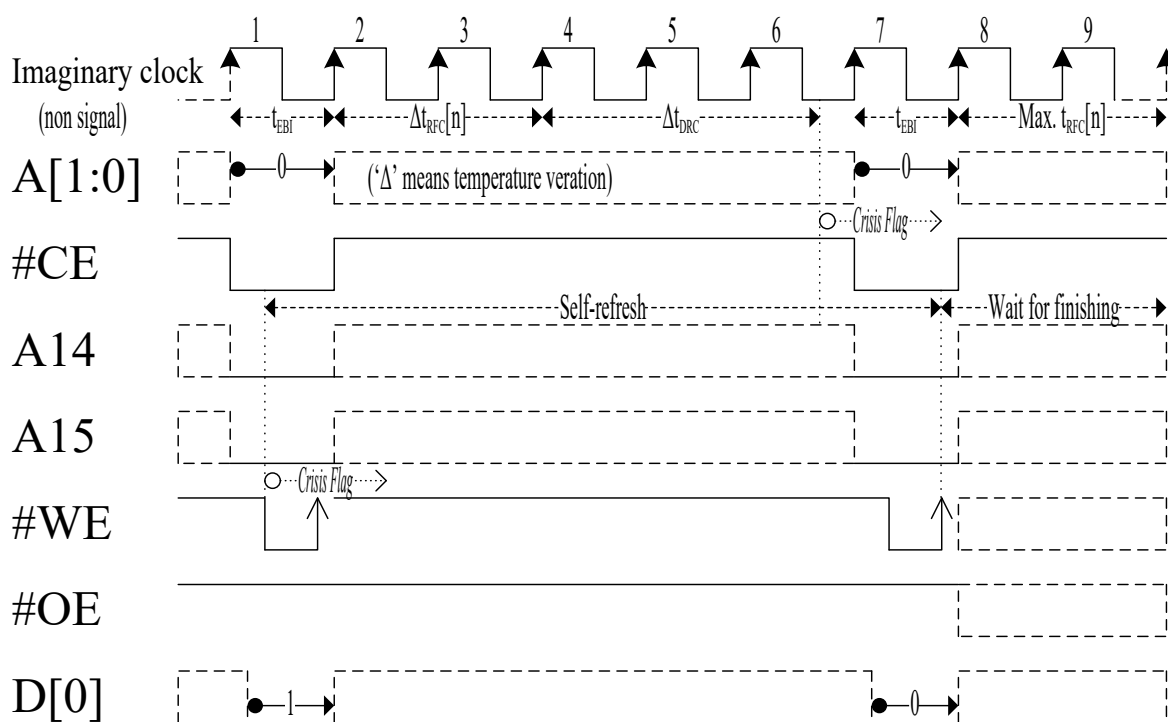
■ Auto Refresh



■ Chip Information and Chip Configuration



■ Self-Refresh Entry and Self-Refresh Exit





## EBI DRAM

Applying to a dynamic random-access memory without refresh command. Its interface is low pin count, and it such likes as the pseudo-SRAM, but the performance is higher.

Other items please refer to SPMI DRAM.

## Operation Time of Accessing

### ■ The device refresh parameters

tDRC: decided by the struct of the storage cell, the process technology, and the 'n'

$$t_{RFC} = t_{RP} + t_{RCD}^{REF} \left[ t_{RCD}^{REF} \geq t_{RCD} \right]$$

### ■ The time of random access (tRACC) with data amount (DA)

$$t_{RACC} = t_{RFC} + t_{RCD} + t_{NAI} * DA + t_{EBI} * (2 + DA)$$

### ■ The time of burst access (tBACC) with data amount (DA)

$$t_{BACC} = t_{RFC} + t_{RCD} + t_{NAI} * DA + t_{EBI} * 3 + t_{ACC} * (DA - 1)$$

## Command Set

Function	A[15:14]	A[r-1:0]	D[7:0]
Single Bank Precharge;	01	Row Address	Bank Address
Random Access;	01	Column Address* <sup>1</sup>	Byte
Function End	00	X	X
Single Bank Precharge;	01	Row Address	Bank Address
Synchronization Burst Access* <sup>2</sup> ;	01	Column Address* <sup>1</sup>	Byte
Function End	00	X	X
Read Chip Information	00	Page Number* <sup>3</sup>	V (hardware fixed)
Write Chip Configuration	00	Page Number* <sup>3</sup>	V (power on reset)
NOTE 1: the device first receives the row address, and then receives the column address (A[c-1:0]) after.			
NOTE 2: rolling column address.			
NOTE 3: using A[1:0] only.			

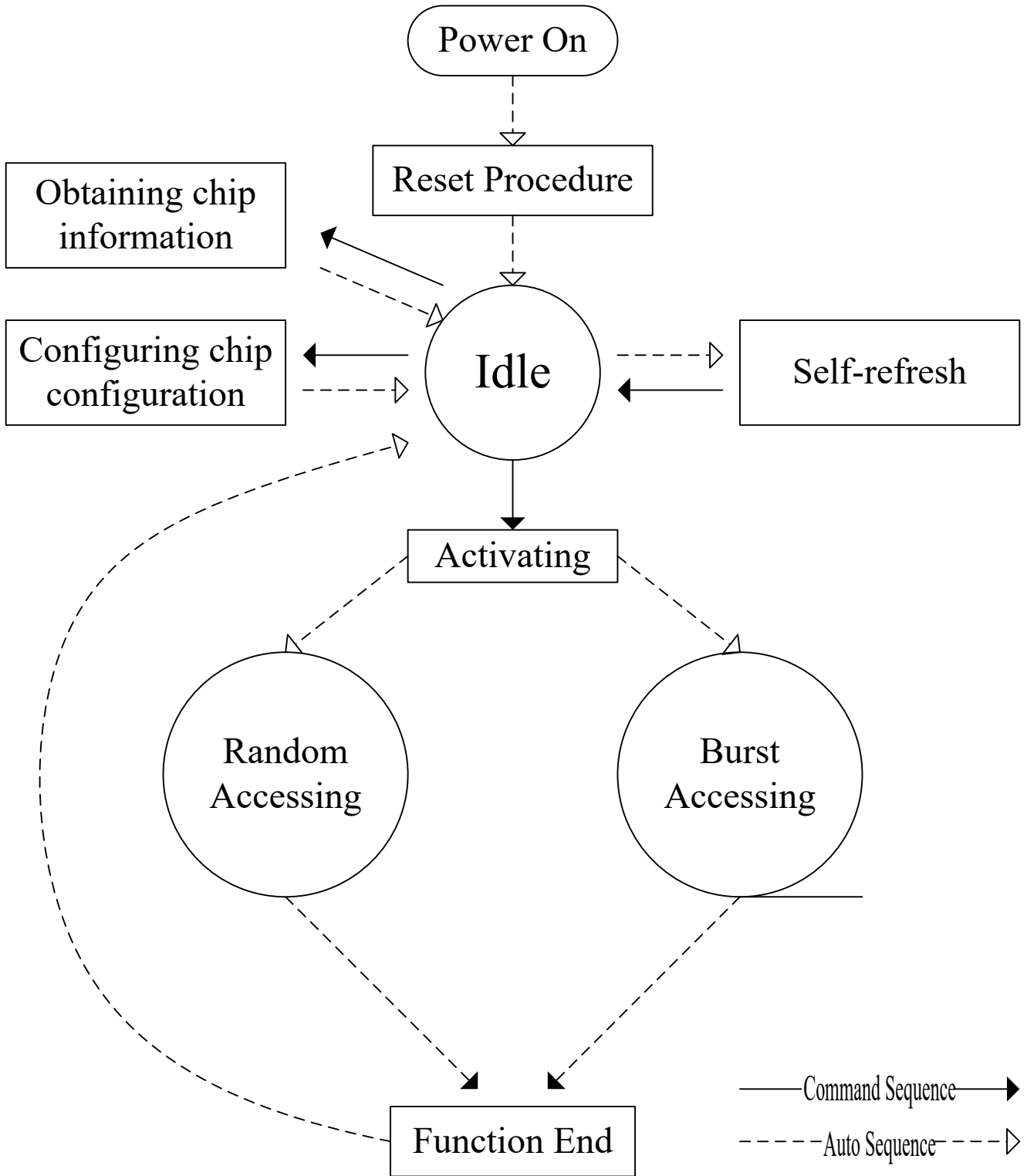
### Chip Information

Please refer to SPMI DRAM.

### Chip Configuration

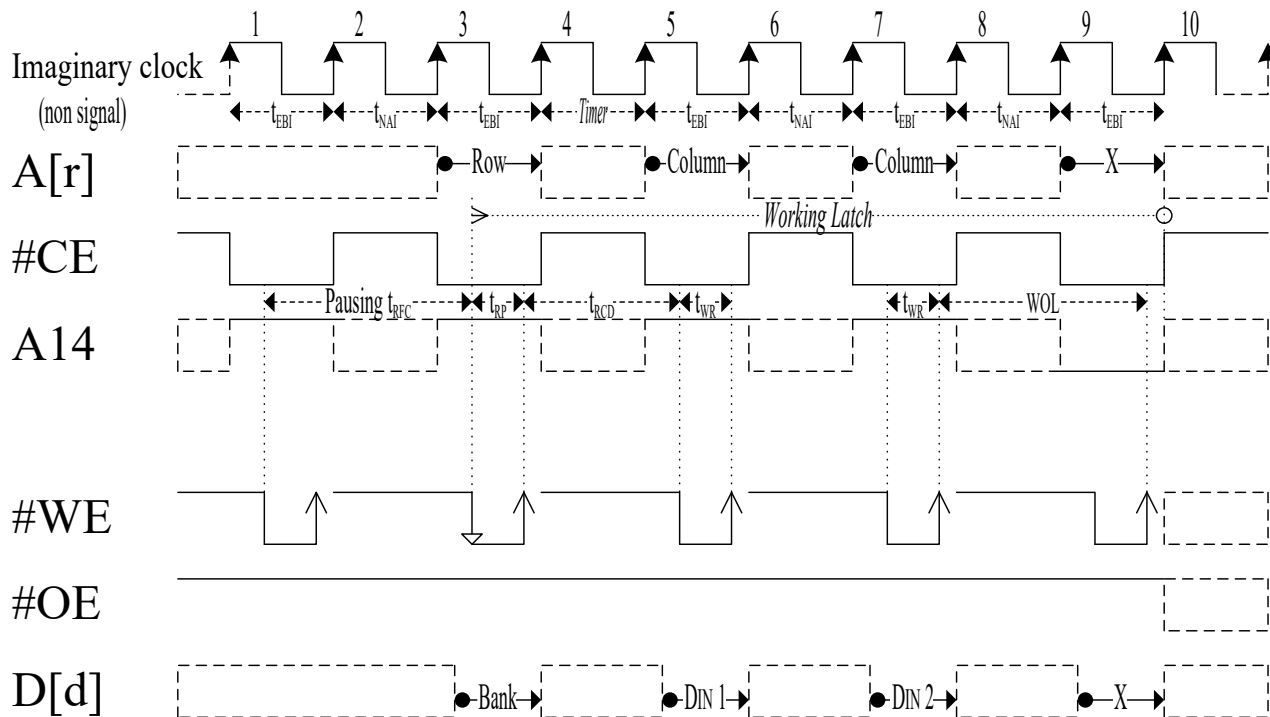
Please refer to SPMI DRAM, this chip configuration removes the self-refresh configuration.

## Simplified State Diagram

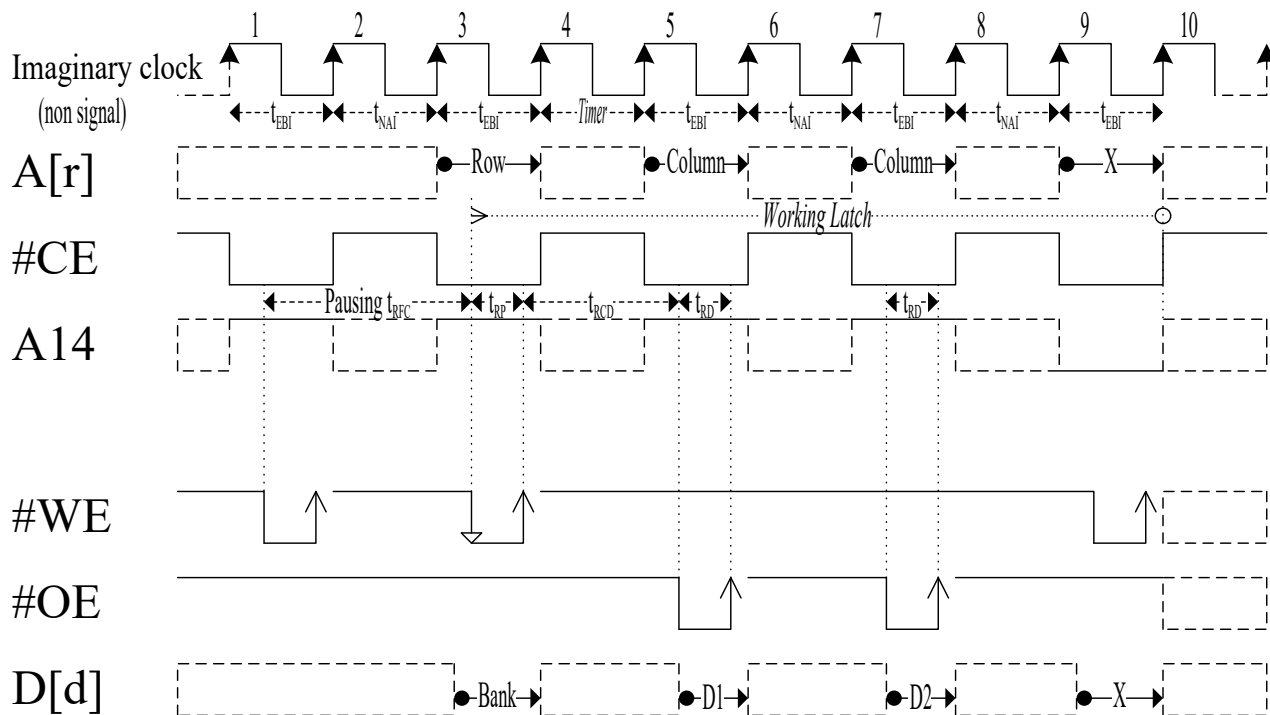


## Timing Diagram

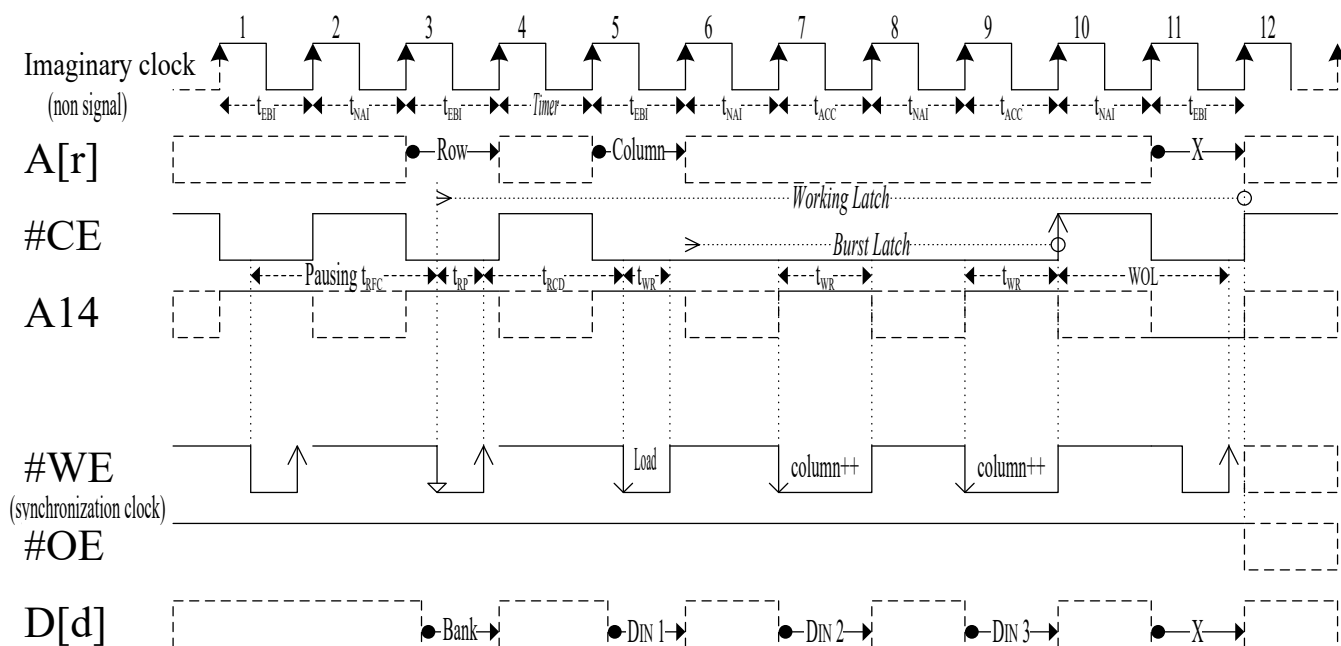
### ■ Random Write



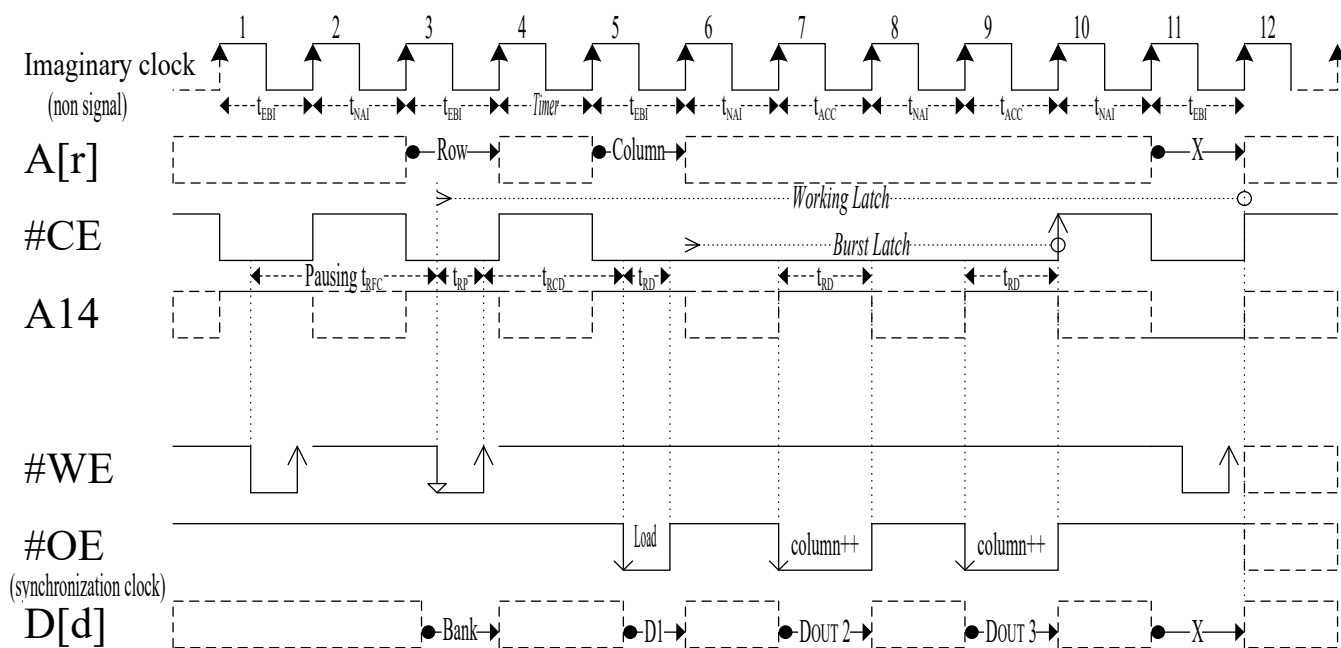
### ■ Random Read



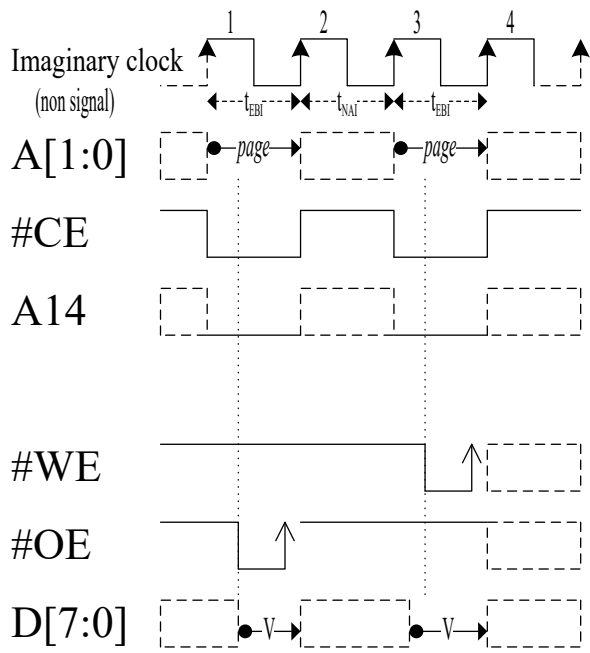
■ Synchronization Burst Write



■ Synchronization Burst Read



## ■ Chip Information and Chip Configuration



## SPMI NAND

Applying to the flash memory of NAND type.

### Command Set

Function	A[19]	A[18:0]	D[7:3]	D[2:0]
Data Access	1	Column Address <sup>*1</sup>	Upper bits	Lower
Random Access	1	[Block], A[0]=0	LUN, Plane	0
Synchronization Burst Access <sup>*2</sup>	1	[Block], A[0]=1	LUN, Plane	0
Block Erase (one block)	1	Block, A[0]=0	LUN, Plane	1
Block Erase all Planes	1	Block, A[0]=1	LUN, X	1
Page Read / Page Program (one page)	1	Block, Page	LUN, Plane	2 / 3
Page Read all Planes / Page Program all Planes	1	Block, Page	LUN, D[3]=0 / 1	4
Write to Reset	1	X	X	X
Read Status; reply: Busy / Ready	1	X	X	D[0] 1 / 0
Function End	0	X	X	X
Read Chip Information	0	Page Number <sup>*3</sup>	V (hardware fixed)	
Write Chip Configuration	0	Page Number <sup>*3</sup>	V (power on reset)	
NOTE 1: the device first receives the block and page address, and then receives the column address after.				
NOTE 2: rolling column address.				
NOTE 3: using A[1:0] only.				

**Chip Information**

D[7:5]	D[4:2]	D[1:0]	A[1:0]
<b>Size of a page, and a block</b>	<b>Number of blocks</b>	<b>Number of LUN</b>	<b>Info. Page</b>
000: 256, 64KB (legacy)	000: 16	00: 1 (legacy)	00: page 0
001: 512, 128KB	001: 32	01: 2	
010: 1024, 256KB	010: 64	10: 4	
011: 2048, 512KB	011: 128	11: 8	
100: 4096, 1024KB	100: 256		
101: 8192, 2048KB	101: 512		
110: 16384, 4096KB	110: 1024		
111: 32768, 8192KB	111: 2048		

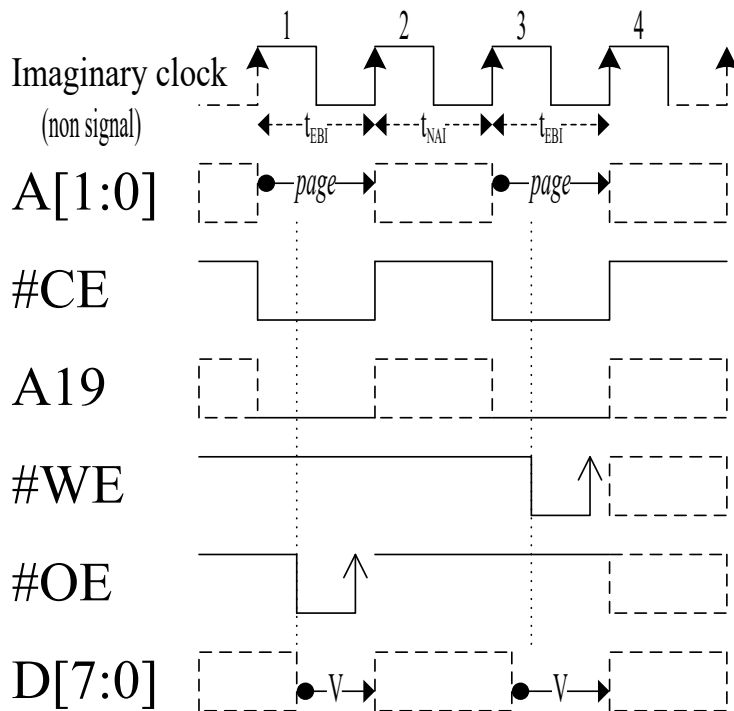
D[7:6]	D[5:3]	D[2:0]	A[1:0]
<b>Number of planes</b>	<b>Erase time (typical)</b>	<b>Program time (typical)</b>	<b>Info. Page</b>
00: 1 (legacy)	000: 100us	000: 10us	01: page 1
01: 2	001: 250us	001: 25us	
10: 4	010: 500us	010: 50us	
	100: 1ms	100: 100us	
	101: 2ms	101: 200us	
	110: 2.5ms	110: 250us	
	111: 5ms	111: 500us	

**Chip Configuration**

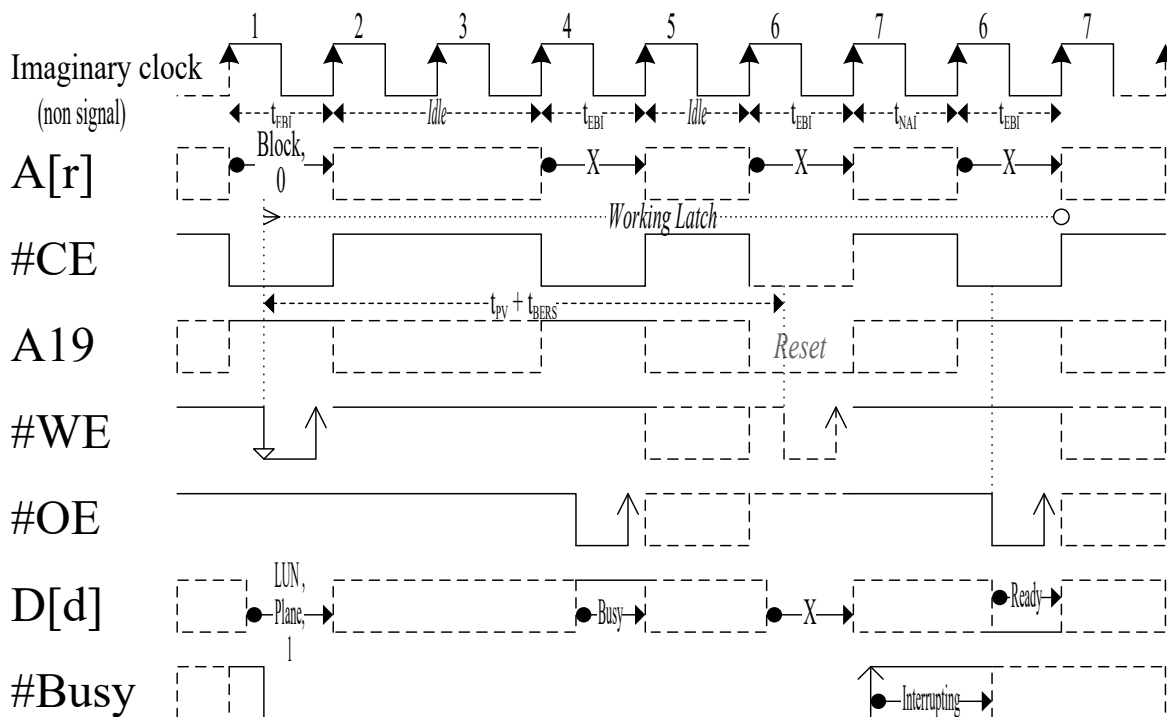
D[7:0]	A[1:0]
<b>Null</b>	<b>Config page</b>
0	00: page 0

## Timing Diagram

### ■ Chip Information and Chip Configuration

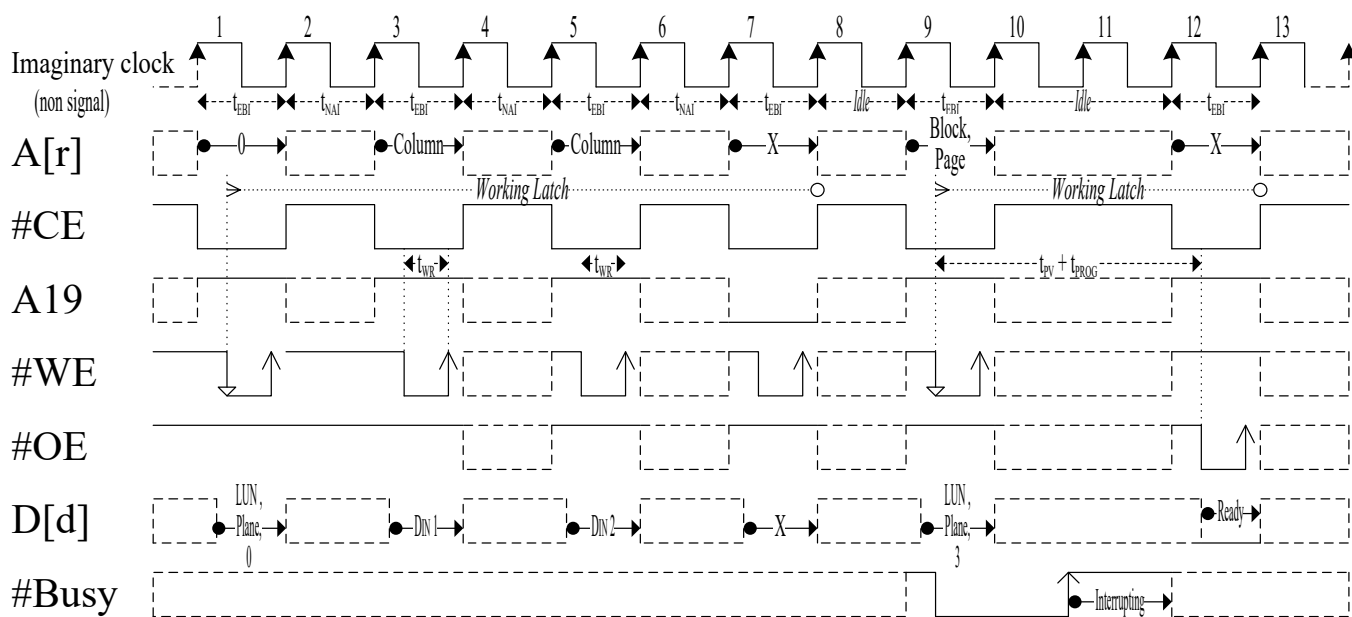


### ■ Block Erase

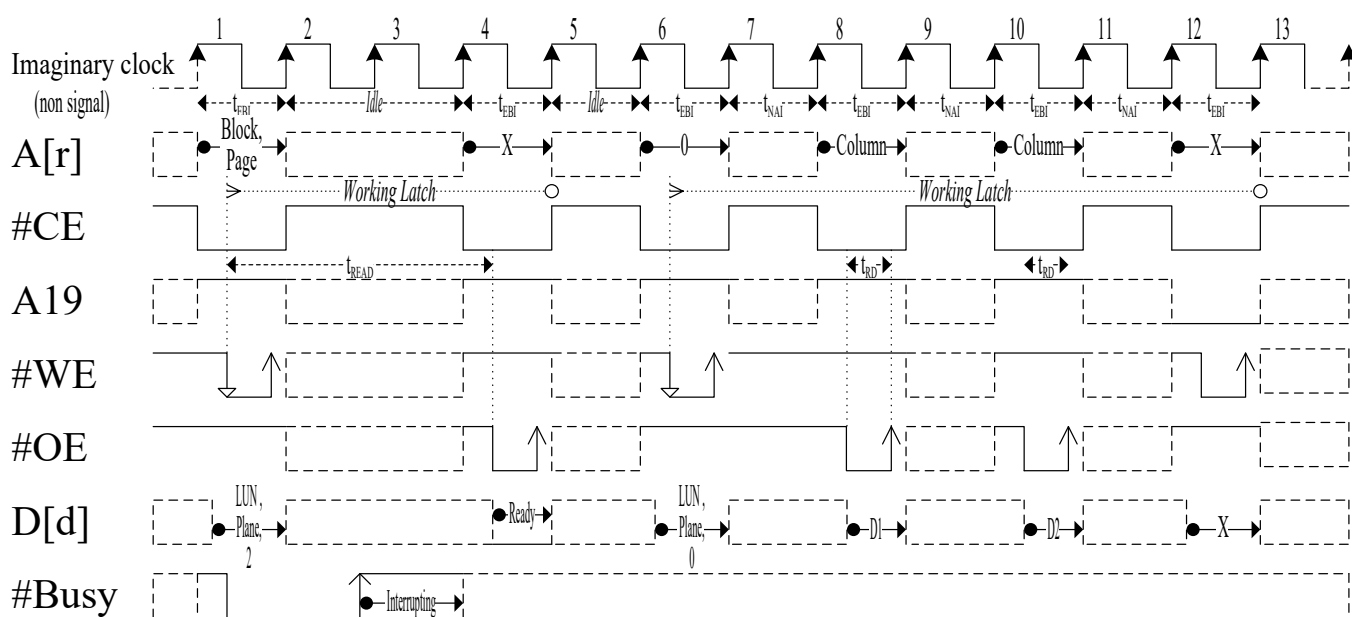




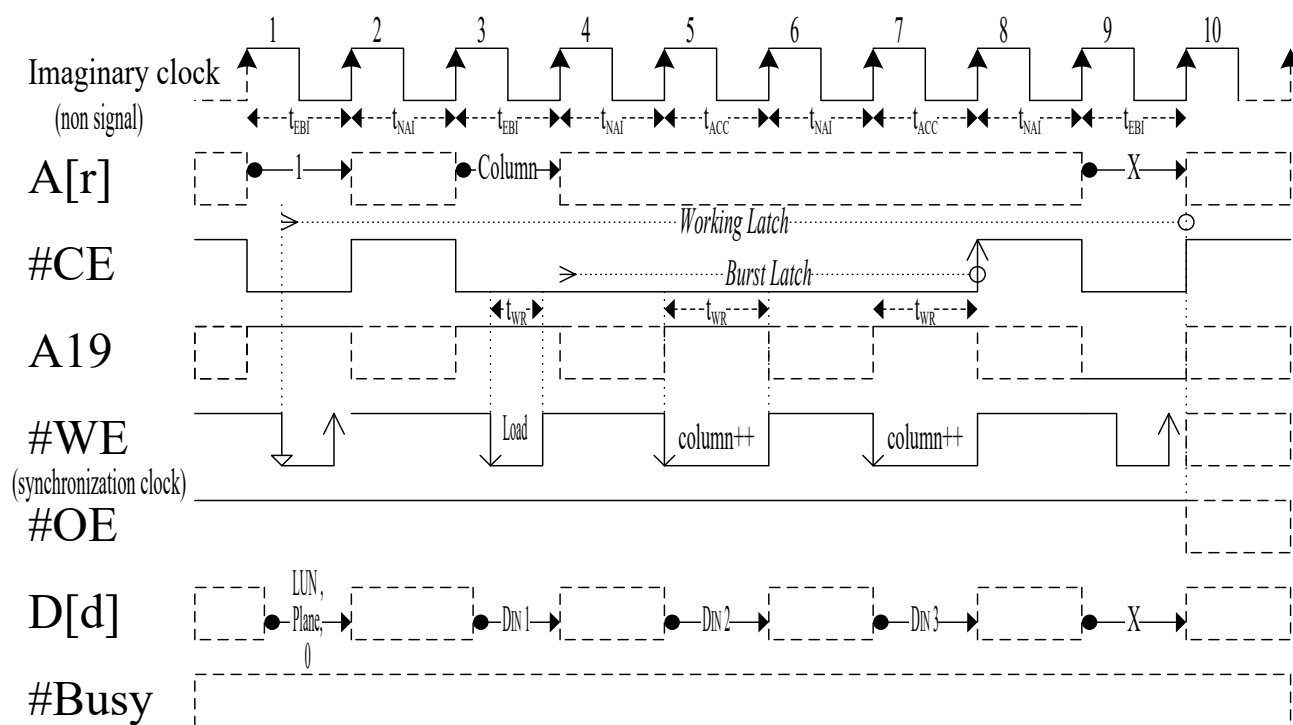
■ Random Write and Page Program



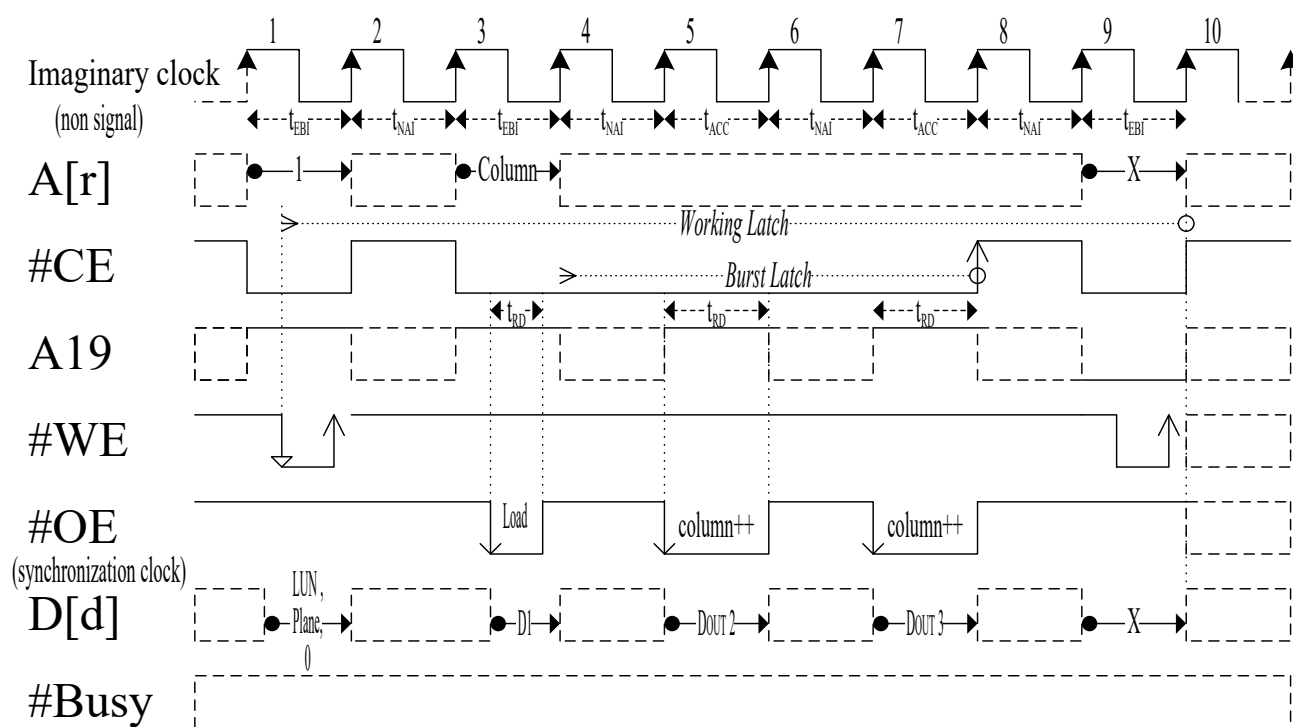
■ Page Read and Random Read



■ Synchronization Burst Write



■ Synchronization Burst Read



# Release Note

## Table of Release Note

Version	Release Date	Release Note
1.0	2020-05-11	First formal version.
1.1	2020-05-18	According to the asynchronous SRAM chip which can select data width is single byte or double byte, the package ball-out can add the #UB and #LB.
1.2	2020-07-27	To add SPMI DRAM versus DDR2 SDRAM.
1.3	2020-08-03	<ol style="list-style-type: none"> <li>1. To beautify SPMI DRAM versus DDR2 SDRAM.</li> <li>2. To beautify timing diagrams and correct symbols on them.</li> <li>3. To correct the operation time of accessing.</li> <li>4. To correct some error words.</li> </ol>
1.4	2020-08-24	<ol style="list-style-type: none"> <li>1. To define clearly, the symbols CK and #CK are reserved signals.</li> <li>2. To rename the "Speed Write" becoming "Fast Write".</li> <li>3. To add a write mode in MRS, and remove the Fast Write from command set.</li> <li>4. To rename the "Write" in timing diagram of SPMI DRAM.</li> <li>5. To rename the "Operation Time of Accessing and Refreshing" in SPMI SRAM.</li> <li>6. To change the number of the Fast Write in SPMI SRAM.</li> <li>7. To rename the "SPMI NAND Flash Memory".</li> <li>8. To change the number of the Random Write in SPMI NAND.</li> <li>9. To correct some symbols in timing diagram of SPMI NAND.</li> <li>10. To add an approach of a bridge board.</li> </ol>
1.5	2021-04-12	<ol style="list-style-type: none"> <li>1. To correct the command set and the timing diagram of SPMI DRAM; and to exchange the read and write timing diagram (SPMI SRAM), by the way.</li> <li>2. To modify the Platform Hardware Architecture.</li> <li>3. To modify the architecture of SPMI DRAM, and SPMI SRAM.</li> </ol>
1.6	2021-08-02	<ol style="list-style-type: none"> <li>1. Fixed some bugs of all timing diagram.</li> <li>2. Fixed command set of burst access.</li> <li>3. Merge SPMI DRAM with SPMI SRAM.</li> </ol>
1.7	2021-09-13	<ol style="list-style-type: none"> <li>1. Fixed some bugs of all timing diagram.</li> <li>2. Remove the power down command in SPMI DRAM.</li> <li>3. Modify the Mode Register.</li> <li>4. Modify the Operation Time of Accessing and Refreshing.</li> </ol>
1.8	2021-09-20	<ol style="list-style-type: none"> <li>1. Modify the command set and the function number in SPMI DRAM.</li> <li>2. Modify the quantity of periodic refresh command.</li> <li>3. Modify the function name in SPMI NAND.</li> </ol>
1.9	2021-09-27	Modify the SDRAM bridges.
1.10	2021-11-22	Modify the SPMI DRAM versus [DDR-n] SDRAM.

1.11	2022-02-07	<ol style="list-style-type: none"> <li>1. Fixed the figures (Platform Hardware Architecture, and SPMI DRAM versus [DDR-n] SDRAM).</li> <li>2. Fixed the command set of SPMI DRAM.</li> </ol>
2.0	2022-03-28	<p>To upgrade SPMI DRAM and SPMI NAND.</p> <p>To reduce GPIO operation times (switching GPIO is usually slower).</p>
3.0	2022-04-08	<p>To upgrade SPMI DRAM and SPMI NAND.</p> <p>To remove all GPIO (it is not fast on advanced hardware and software platforms).</p>
3.1	2022-07-25	<ol style="list-style-type: none"> <li>1. To add EBI DRAM.</li> <li>2. Fixed all of the Package Ball-out.</li> <li>3. To beautify the Timing Diagram of EBI.</li> <li>4. To beautify all of the Timing Diagram.</li> </ol>
3.2	2022-08-29	<ol style="list-style-type: none"> <li>1. To add DDR3 SDRAM package mapping table.</li> <li>2. The ALE is no more an option on SPMI NAND.</li> <li>3. To redefine the tDACC and tBACC, and tDACC is changed to tRACC.</li> <li>4. To shift the location of Operation Time of Accessing.</li> </ol>
3.3	2022-09-26	<ol style="list-style-type: none"> <li>1. To add Simplified State Diagram.</li> <li>2. Modify Chip Information.</li> </ol>
3.4	2022-10-10	<ol style="list-style-type: none"> <li>1. Modify the waveforms of burst write and burst read.</li> <li>2. Modify the Simplified State Diagram.</li> </ol>